A PHYSICAL LARGE SIGNAL Si MOSFET MODEL FOR RF CIRCUIT DESIGN

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ABSTRACT

A new physically based Si MOSFET large signal model, BSIM3v3, developed by UC Berkeley, has been evaluated for high-frequency mixed-signal circuit analysis in a frequency domain, harmonic balance simulator. The model is validated using simulated RF power characteristics of automatic load pull measurement at different bias and matching conditions.

I. INTRODUCTION

Recent advancement of process technology and device design has allowed Si MOSFETs to be applied successfully to RF circuits, like power amplifiers and mixers [1] [2]. As the trend progresses, it will be possible to integrate RF circuits with base band CMOS circuits. Si MOSFETs thus become attractive candidates for low cost, high volume mobile phone systems operating at 1 to 2 GHz. To shorten the design cycle and ensure required circuit performance, an accurate large-signal device model for frequency domain harmonic balance circuit simulator is needed. However, most existing MOSFET models, such as Berkeley SPICE Level 3 and BSIM2 (Berkeley Short-channel Insulated gate field effect transistor Model 2) are inadequate because they use piece-wise continuous functions to model the terminal I-V characteristics [3]. This approach can cause serious convergence problems in simulating mixed-signal circuits or complex digital circuits. To solve this problem, various techniques such as adding a non-linear resistor to "force fit" the drain current [4] or using a look-up table for I-V relations [5] have been developed. Both of these approaches have limited application because they are not physically based and are only accurate "simulating" the measured devices.

In 1995, the University of California at Berkeley released a new MOSFET model, BSIM3v3 [6], which is supported as an industry standard by a Compact Model Council associated with the Electronic Industry Association (EIA). BSIM3v3 is capable of modeling deep sub-micron devices and uses a single, smooth and continuous function to simulate the terminal currents of the device over all bias ranges [7] [8]. The high order derivatives of current with respect to voltage calculated by BSIM3v3 are also continuous. This in turns improves the convergence of the circuit simulator. For RF applications, it was desirable to incorporate this model into a harmonic balance simulator and validate the accuracy of the model at RF frequencies. We have successfully accomplished this with HP-EEsof Libra via user-defined model elements. Furthermore, we have compared the simulated and measured data of 900 MHz automatic load-pull measurements at class A, class AB and class B bias conditions. By showing good agreement between the simulated and measured output power (P_{out}), transducer power gain (G_T) and power add-up efficiency (PAE), the BSIM3v3 model was qualified as an accurate large signal model for high frequency (RF) mixed-signal MOSFET circuit analysis.

II. MODEL PARAMETER EXTRACTION

The test device was a RF power MOSFET, which was fabricated by a modified version of Texas Instruments' 1.0 μm BiCMOS Technology [9]. The gate finger width is 50 μm and the total gate width is 2 mm (40 fingers). An extended lightly doped drain (LD) region was used to increase the drain to source breakdown voltage (BV_{DSS}) to larger than 20 V. Most of the device parameters, except process related parameters like SiO_2 thickness and channel doping, were determined by methods similar to the one used in

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[4]. The device model parameters controlling the DC characteristics were first determined by analyzing the I_D-V_{DS} and I_D-V_{GS} data. The measured 0.2 to 6.0 GHz s-parameters were then used to extract the device model parameters associated with device charges and capacitance.

Although BSIM3v3 was developed for symmetrical structures, the effects of the LD region on device characteristics could be accounted for by adding an external drain resistor and choosing proper value of the drain to bulk junction capacitance. Under normal operating conditions ($V_{DS} \leq 4.8$ V), the value of the external drain resistor can be considered as a constant. The equivalent circuit of the device under test is shown in Fig. 1. Note that the body is always connected to the intrinsic source.

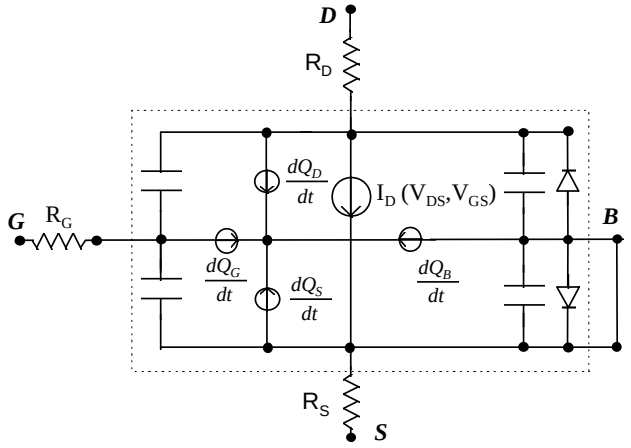
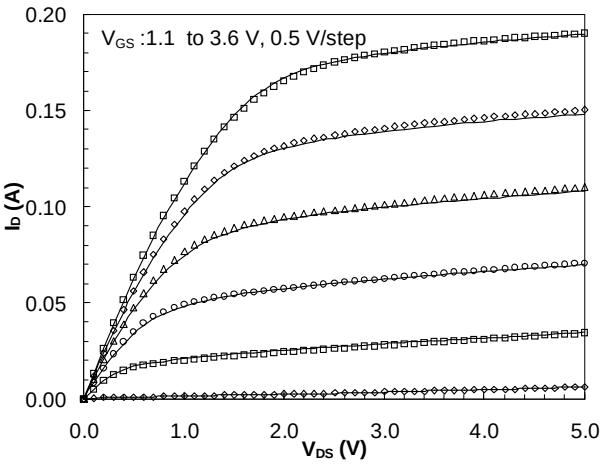
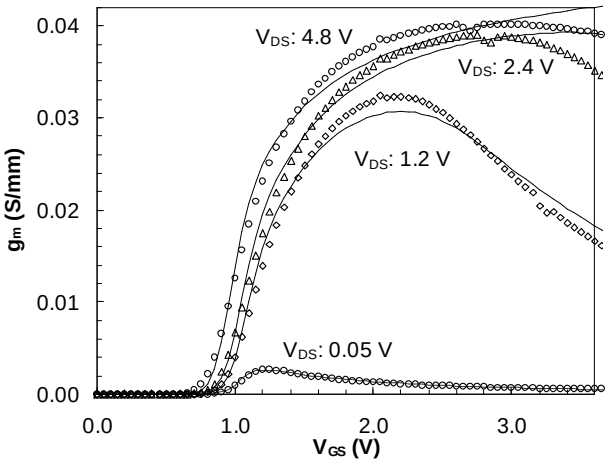


Fig. 1. The equivalent circuit of the RF power MOSFET. The intrinsic device lies inside the dotted line.

As shown in Fig. 2 and Fig. 3, the measured and simulated I_{DS} (g_m) *vs.* V_{DS} (V_{GS}) and s-parameters of the asymmetrical RF (LD)MOSFET were in close agreement. The 6 GHz upper limit of the s-parameters was chosen because it was higher than the third harmonic of 1.9 GHz. Thus a device model accurate up to 6 GHz is adequate for designing RF circuits operating at or under 1.9 GHz, which covers most of the commercial wireless applications.

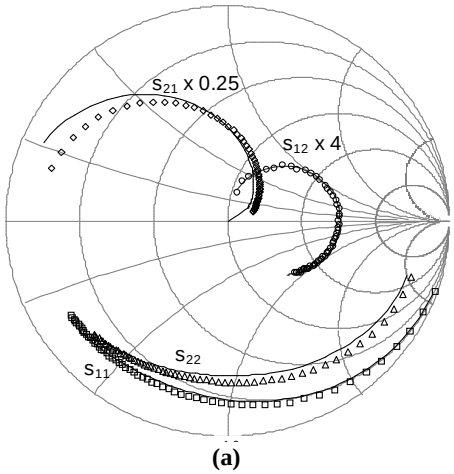


(a)

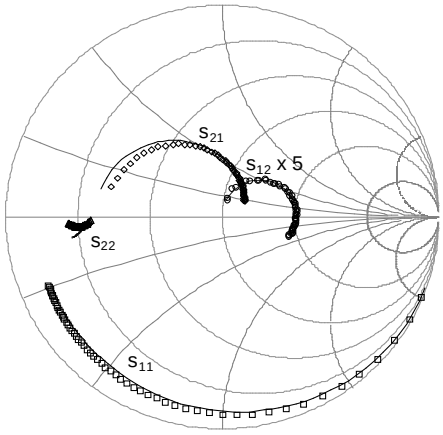


(b)

Fig. 2. Measured (open symbols) and simulated (lines) (a) I_D *vs.* V_{DS} and (b) g_m *vs.* V_{GS} of a 2 mm RF MOSFET.



(a)

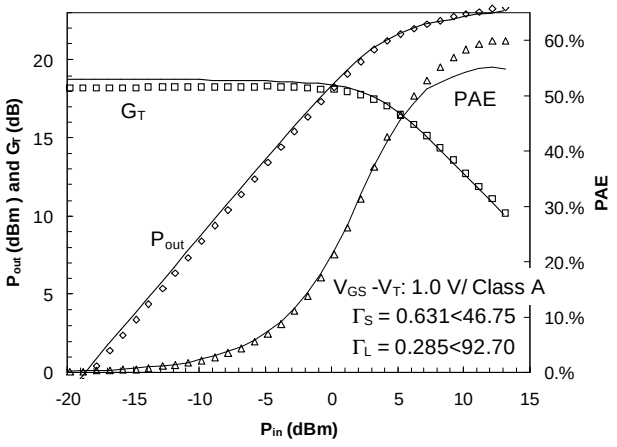


(b)

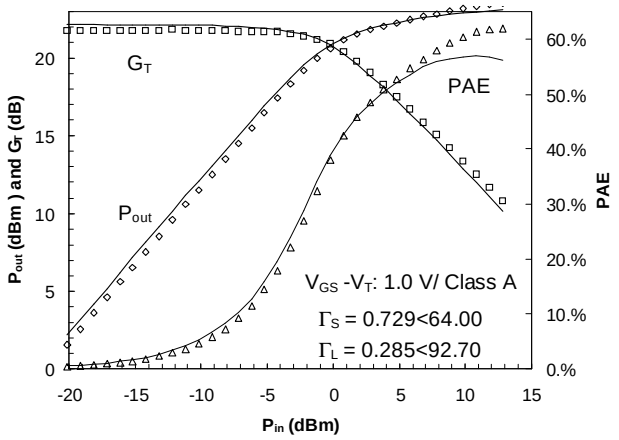
Fig. 3. Measured (open symbols) and calculated (lines) 0.3 to 6.0 GHz s-parameters at (a) V_{DS}: 4.8V, V_{GS}: 1.1V , (b) V_{DS}: 1.2V, V_{GS}: 3.6 V.

III. VALIDATION OF MODEL

After the model parameters of the RF MOSFET were extracted, P_{out}, G_T and PAE were simulated based on automatic load/source pull measurements at 900 MHz and V_{DD} = 4.8 V. The comparison between the measured and simulated data were shown in Figure 4. The simulated RF power characteristics were very close to the measured ones at bias conditions ranging from class A to class B, even after the device was driven more than 6 dB into compression. At the same bias, the BSIM3v3 model could also accurately predict the output power and efficiency at different matching conditions.



(a)



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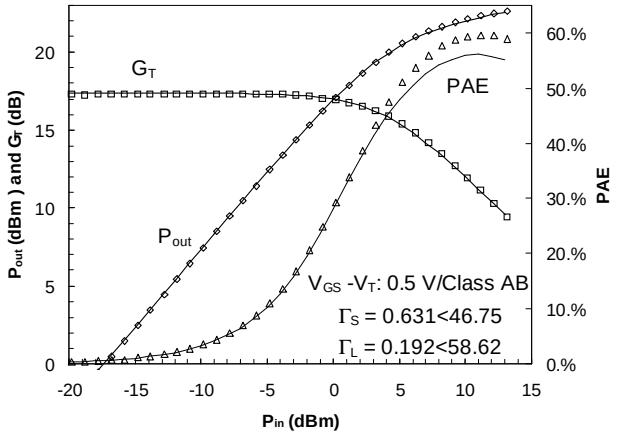

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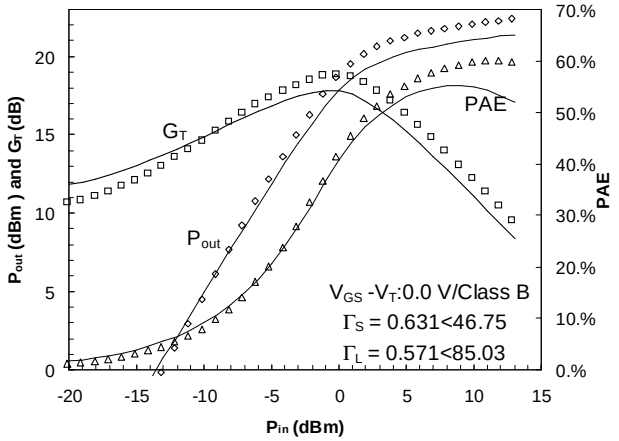

(d)

Fig. 4. Measured (open symbols) and simulated (lines) 900 MHz power characteristics of a 2 mm RFMOSFET in different bias and matching conditions. Γ_S (Γ_L) is the input (output) tuner impedance and V_{DD} = 4.8 V.

On the other hand, the Level 3 MOSFET Model, which is a standard model in Libra, failed to converge when the device was saturated at high input power levels due to discontinuities between its piece-wise continuous current equations.

It should be pointed out that the RF MOSFET was biased in "sliding class A" condition [10] in Fig. 4(a) and 4(b), i.e. the device worked in class A at low RF input power level and went into class AB when the RF input power level was high. The PAE was therefore larger than 50% when the device was saturated.

IV. CONCLUSION

The good agreement between the simulated and measured data validate the accuracy of the parameter extraction procedure and strongly suggest the possibility of using BSIM3v3 in high-frequency mixed-signal circuit simulations. The ability of the model to simulate the device operating in saturation mode further demonstrated the potential of the model. It can also be used in optimizing the layout and device structure because current and charge are calculated based on physical equations and parameters. Already fully supported by the EIA Compact Model Council as the standard MOSFET model for VLSI circuit design, BSIM3v3 should be also considered as the standard model for RF circuit simulation.

ACKNOWLEDGMENT

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